

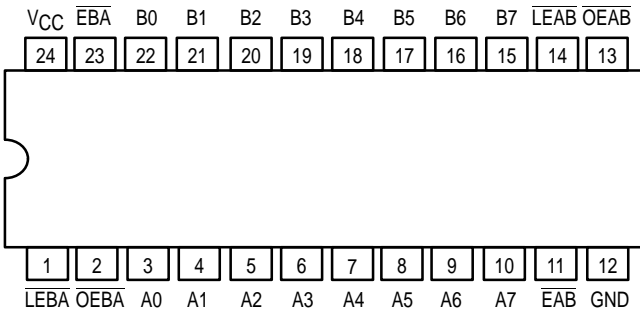


OCTAL REGISTERED TRANSCEIVER, NON-INVERTING, 3-STATE

The MC74F543 Octal Registered Transceivers contain two sets of data flowing in either direction. Separate Latch Enable (\overline{LEAB} , \overline{LEBA}) and Enable (\overline{OEAB} , \overline{OEBA}) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The MC74F543 has a noninverting data path. The A outputs are guaranteed to sink 20 mA while the B outputs are rated for 64 mA.

- Combines 74F245 and 74F373 Type Functions in One Chip
- 8-Bit Octal Transceiver
- Non-Inverting
- Back-to-Back Registers for Storage
- Separate Controls for Data Flow in Each Direction
- Glitchless Outputs During 3-State Power Up or Power Down Operation
- High Impedance Outputs in Power Off State
- A Outputs Sink 24 mA and Source 3.0 mA
- B Outputs Sink 64 mA and Source 15 mA
- See F544 for Inverting Version
- ESD Protection > 4000 Volts

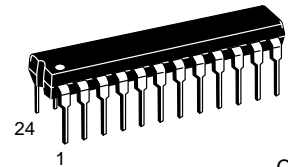
PIN ASSIGNMENT



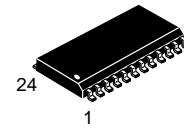
MC74F543

OCTAL REGISTERED
TRANSCEIVER,
NON-INVERTING, 3-STATE

FAST™ SCHOTTKY TTL



N SUFFIX
PLASTIC
CASE 724-03



DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-3.0/-15	mA
I _{OL}	Output Current — Low	74			24/64	mA

MC74F543

FUNCTION TABLE

Inputs				Outputs	Status
$\overline{OE}X\overline{X}$	$\overline{E}X\overline{X}$	$\overline{LE}X\overline{X}$	Data		
H	X	X	X	Z	Outputs disabled
L	H	L	l	Z	Outputs disabled
L	H	L	h	Z	Data latched
L	L	H	l	L	Data latched
L	L	H	h	H	Data latched
L	L	L	L	L	Transparent
L	L	L	H	H	Transparent

H = HIGH voltage level; h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}X\overline{X}$ or $\overline{E}X\overline{X}$ (XX = AB or BA); L = LOW Voltage Level; l = LOW state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}X\overline{X}$ or $\overline{E}X\overline{X}$ (XX = AB or BA); X = Don't care; Z = HIGH impedance state.

FUNCTIONAL DESCRIPTION

The MC74F543 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{E}A\overline{B}$) Input must be LOW in order to enter data from A0–A7 or take data from B0–B7, as indicated in the Function Table. With $\overline{E}A\overline{B}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LE}A\overline{B}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH

transition of the $\overline{LE}A\overline{B}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{E}A\overline{B}$ and $\overline{OE}A\overline{B}$ both LOW, the 3-State B output buffers are active and reflects the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{E}B\overline{A}$, $\overline{LE}B\overline{A}$, and $\overline{OE}B\overline{A}$ inputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions		
			Min	Typ	Max				
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage		
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage		
V_{IK}	Input Clamp Diode Voltage			-0.73	-1.2	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$		
V_{OH}	Output HIGH Voltage	A0–A7	74	2.4		V	$I_{OH} = -3.0 \text{ mA}$	$V_{CC} = 4.5 \text{ V}$	
				2.7	3.4			$V_{CC} = 4.75 \text{ V}$	
		B0–B7	74	2.0		V	$I_{OH} = -15 \text{ mA}$	$V_{CC} = 4.5 \text{ V}$	
V_{OL}	Output LOW Voltage	A0–A7	74		0.35	0.5	V	$I_{OL} = 24 \text{ mA}$	$V_{CC} = \text{MIN}$
		B0–B7	74		0.4	0.55	V	$I_{OL} = 64 \text{ mA}$	
I_{IH}	Input HIGH Current	I/O Pins				1.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 5.5 \text{ V}$	
		Control Pins				100	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
						20		$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
I_{IL}	Input LOW Current	$\overline{E}A\overline{B}$, $\overline{E}B\overline{A}$				-1.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5 \text{ V}$	
		Other Inputs				-0.6			
I_{OZH}	Off-State Output Current, High-Level Voltage Applied					70	μA	$V_{CC} = \text{MAX}$	$V_{OUT} = 2.7 \text{ V}$
						1.0			mA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied					-600	μA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0.5 \text{ V}$	
I_{OS}	Output Short Circuit Current (Note 2)	A_n Outputs		-60		-150	mA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0 \text{ V}$	
		B_n Outputs		-100		-225			
I_{CC}	Total Supply Current	I_{CCH}			70	100	mA	$V_{CC} = \text{MAX}$	
		I_{CCL}			95	125			
		I_{CCZ}			95	125			

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

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AC ELECTRICAL CHARACTERISTICS

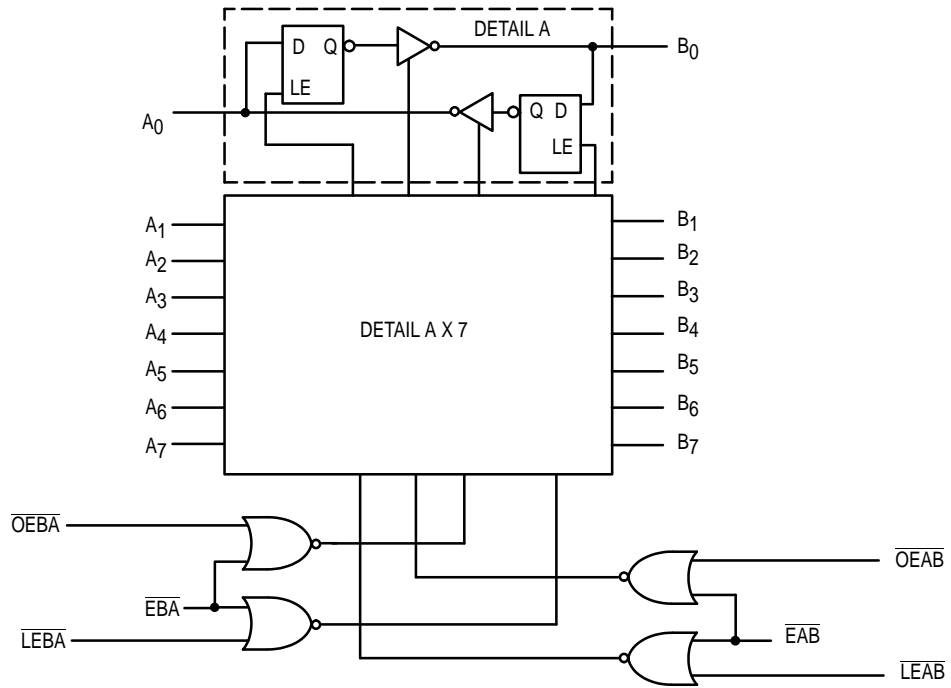
Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	70	100		70		MHz
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A _n to B _n or B _n to A _n	3.0 3.0	5.5 5.0	7.5 6.5	3.0 3.0	8.5 7.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEB _A to A _n	4.5 4.5	8.5 8.5	11 11	4.5 4.5	12.5 12.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEA _B to B _n	4.5 4.5	8.5 8.5	11 11	4.5 4.5	12.5 12.5	ns
t _{PZH} t _{PZL}	Output Enable Time to OE _B _A or OE _A _B to A _n or B _n EB _A or E _A _B to A _n or B _n	3.0 4.0	7.0 7.5	9.0 10.5	3.0 4.0	10 12	ns
t _{PHZ} t _{PLZ}	Output Disable Time to OE _B _A or OE _A _B to A _n or B _n EB _A or E _A _B to A _n or B _n	2.5 2.0	6.0 5.5	8.0 7.5	2.5 2.0	9.0 8.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _s (H) t _s (L)	Setup Time, HIGH or LOW A _n or B _n to LE _B _A or LE _A _B	3.0 3.0			3.5 3.5			ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW A _n to B _n to LE _B _A or LE _A _B	3.0 3.0			3.5 3.5			ns
t _w (L)	Latch Enable, B to A Pulse Width, LOW	8.0			9.0			ns

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LOGIC DIAGRAM



NOTE:

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.